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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,609	10/02/2003	Susumu Kasukabe	500.43175X00	7923

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EXAMINER	
TANG, MINH NHUT	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,609	KASUKABE ET AL.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/02/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on October 02, 2003 is considered by the examiner.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 6, 13 and 15 are objected to because of the following informalities:

a/ in claim 6, the limitation "each of which has a larger contact area with the wafer than said contact terminal" is vague. For examination purposes, the limitation above is interpreted as -- each of which has a larger contact area with the wafer than contact area of each of said contact terminal --.

b/ Applicant is advised that should claim 13 be found allowable, claim 15 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing

one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakata (U.S.P. 6,215,321).

As to claim 1, Nakata discloses, in Fig. 2, a probe sheet (20) comprising: contact terminals (22b) that get into contact with electrodes (26) provided on a wafer (25); wirings (i.e., metal material filled in each apertures of the thin film 22, herein after metal material) drawn from said contact terminals (22b); and electrode pads (29) electrically connected to said wirings (metal material), wherein a pitch of said electrode pads (29) is wider than a pitch of said contact terminals (22b).

As to claim 2, Nakata discloses in Fig. 2, said contact terminals (22b) are arranged according to an array of peripheral electrodes (26) of semiconductor devices formed on said wafer (25) and wherein said electrode pads (29) are arranged in a grid pattern.

As to claim 3, Nakata discloses in Figs. 5C-5D, a metallic sheet (53), from which at least a part corresponding to signal electrode pads of the electrode pads (29) is removed, is provided.

As to claim 4, Nakata discloses in column 7, lines 21-30, a linear expansion coefficient of said metallic sheet (53) is almost equal to a linear expansion coefficient of said wafer (25).

As to claim 5, Nakata discloses in Figs. 5A-5D, said metallic sheet (29) is a 42 alloy sheet.

As to claim 7, Nakata discloses in Fig. 2, said contact terminals (22b) are created each by using an anisotropically etched hole in a crystalline substrate (22) as a cast.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 8-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kohno et al. (U.S.P. 6,614,246).

As to claim 8, Kohno et al. disclose, in Fig. 1, a probe card comprising: a probe sheet (5) having contact terminals (5a) that get into contact with electrodes provided on a wafer (see column 4, lines 47-48, hereinafter wafer); and a multi-layer wiring substrate (8) on which electrodes (8a), which are electrically connected to said contact terminals

(5a), are provided on a surface opposed to the wafer (wafer), and wherein a pitch of said electrodes (8a) provided on the surface of said multi-layer wiring substrate (8) opposed to the wafer (wafer) is wider than a pitch of said contact terminals (5a).

As to claim 9, Kohno et al. disclose in Fig. 1 (also see Figs. 2A-2C), said contact terminals (5a) are arranged according to an array of peripheral electrodes of semiconductor devices (i.e., chips) formed on the wafer (wafer) and wherein the electrodes (8a) of said multi-layer wiring substrate (8) are arranged in a grid pattern.

As to claim 10, Kohno et al. disclose in Fig. 1, the electrodes (8a) of said multi-layer wiring substrate (8) are provided in a device-opposed-area on said multi-layer wiring substrate (8).

As to claim 11, Kohno et al. disclose in Fig. 1, resistors (i.e., resistor of vias, wires formed in the multi-layer wiring substrate 8) are mounted in the device-opposed area on said multi-layer wiring substrate (8).

As to claim 12, Kohno et al. disclose in Fig. 1, the electrodes (5c) of said contact terminals (5a) and the electrodes (8a) of said multi-layer wiring substrate (8) are electrically connected by a connection part (9) provided almost vertically with respect said multi-layer wiring substrate (8).

As to claims 13 and 15,Kohno et al. disclose in Fig. 1, a connection between the electrodes (5c) of said contact terminals (5a) and the electrodes (8a) of said multi-layer wiring substrate (8) is made via wires (5d, 5e) drawn from the contact terminals (5a), electrode pads (5c) connected to said wires (5d, 5e) and having a pitch wider than a

pitch of said contact terminals (5a), and spring probes (9) electrically connected to said electrode pads (5c).

As to claim 14, Kohno et al. disclose in Fig. 1, said spring probes (9) are removable.

As to claim 16, Kohno et al. disclose in Fig. 1, said probe card has a temperature adjustment function.

As to claim 17, Kohno et al. disclose in Fig. 1, said contact terminals (5a) are each a pyramid-shaped or truncated-pyramid-shaped terminal created by using an anisotropically etched hole in a crystalline substrate (5) as a cast.

As to claim 18, Kohno et al. disclose, in Fig. 1, semiconductor test equipment comprising: a stage (not shown) on which a wafer (wafer) is mounted; and a probe card having contact terminals (5a) that get in contact with electrodes of semiconductor devices (chips) formed on the wafer (wafer) and electrically connected to a tester (not shown) that tests electrical characteristics of the semiconductor devices (chips) wherein said probe card comprises a probe sheet (5) having the contact terminals (5a); and a multi-layer wiring substrate (8) whose electrodes (8a) electrically connected to the contact terminals (5a) are provided on a surface opposed to the wafer (wafer) and wherein a pitch of the electrodes (8a) of said multi-layer wiring substrate (8) provided on the surface opposed to the wafer (wafer) is wider than a pitch of said contact terminals (5a).

As to claim 19, Kohno et al. disclose in Fig. 1, a temperature of the stage and the probe card can both be controlled.

As to claim 20, Kohno et al. disclose in Fig. 1, said contact terminals (5a) are each a pyramid-shaped or truncated-pyramid-shaped terminal created with an anisotropically etched hole in a crystalline substrate (5) as a shape former.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata (U.S.P. 6,215,321) in view of Potter (U.S.P. 6,028,437).

As to claim 6, Nakata discloses all the limitations recited in the claim except for dummy terminals, each of which has a larger contact area with the wafer than contact area of each of said contact terminal, are provided on a surface on which said contact terminals are provided. Potter discloses, in Fig. 1, a probe head assembly comprising

dummy terminals (123), each of which has a larger contact area with the wafer (101) than contact area of each of contact terminal (122, see column 4, lines 11-13), are provided on a surface on which said contact terminals (122) are provided. It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the probe device of Nakata by providing dummy terminals as taught by Potter in order to act as a controlled collapse stops when the probe device is in operation.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Fujimoto et al.	6,784,681	Semiconductor Integrated Circuit Testing System And Method.
Fjelstad et al.	6,586,955	Methods And Structures For Electronic Probing Arrays.
Mori et al.	5,321,453	Probe Apparatus For Probing An Object Held Above The Probe Card.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Minh N. Tang
Primary Examiner
Art Unit 2829
9/17/04